1 Current setup

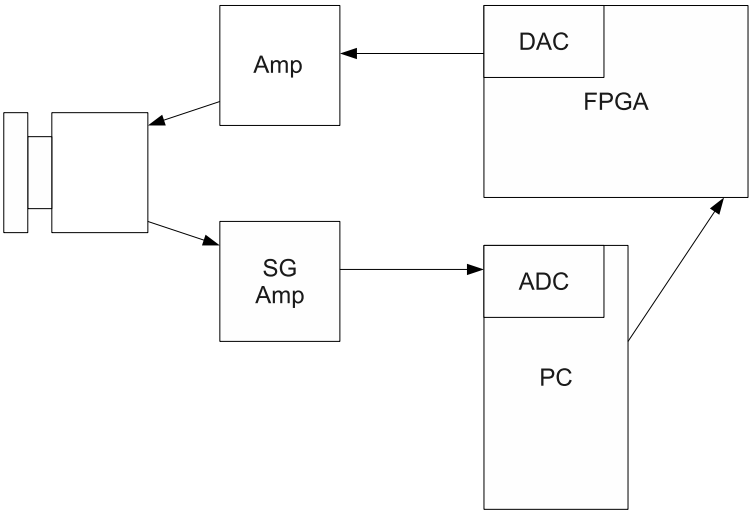

Figure 1: Current setup for modulators

The current setup used for the modulator experiment is based around an FPGA board. The driver card is located on the FPGA where a waveform is written to memory and a module iterates over the memory outputting values to the DAC. Due to the current restrictions of the driver card, the signal must be fed through an amplifier. In this case, the amplifier has unity gain and is only there to boost the current required for a quick transition in the waveform. The strain gauge signal output by the modulator is amplified and sampled by an ADC located within a desktop PC. All analysis is done on the PC. The amplifier used to boost the current is based around two MOSFETs.

2 FPGA/ current setup

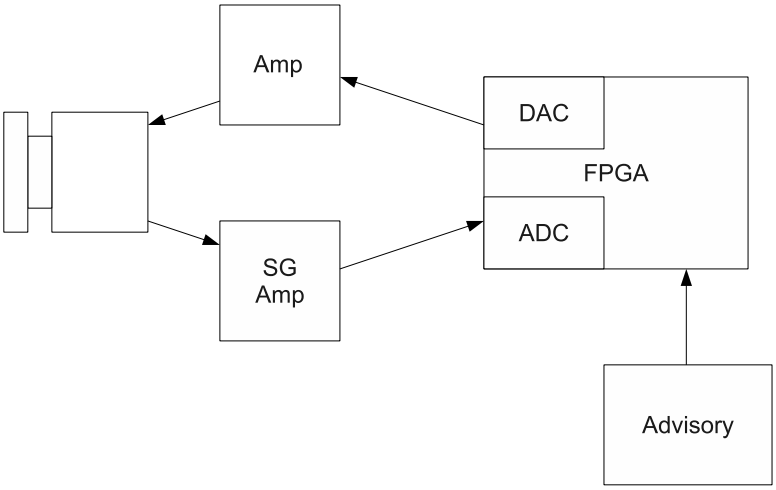

Figure 2: FPGA setup for modulators

In the FPGA based setup, the ADC would be moved onto the FPGA. This setup would only require an amplifier for each channel/ modulator being run. If for some reason, the ADC cannot be located on the FPGA, reverting back to the current setup would be permissible.

The attraction of this setup is, apart from the amplifier, all equipment is on hand and there is ethernet support on the FPGA already. It is limited however in that the current FPGA board can only hold two of the driver cards resulting in only six modulators being run. Due to PCI bus timing, running multiple modulators will have to be verified.

While in working order, this setup will not be able to handle all modulators with the current driver cards. Either new driver cards will have to be obtained or another FPGA board. Getting new driver cards could open the door for a different amplifier that does not have unity gain and possibly getting the driver cards off the PCI bus.

The optimization algorithm could be performed on the FPGA too.

3 SBC setup

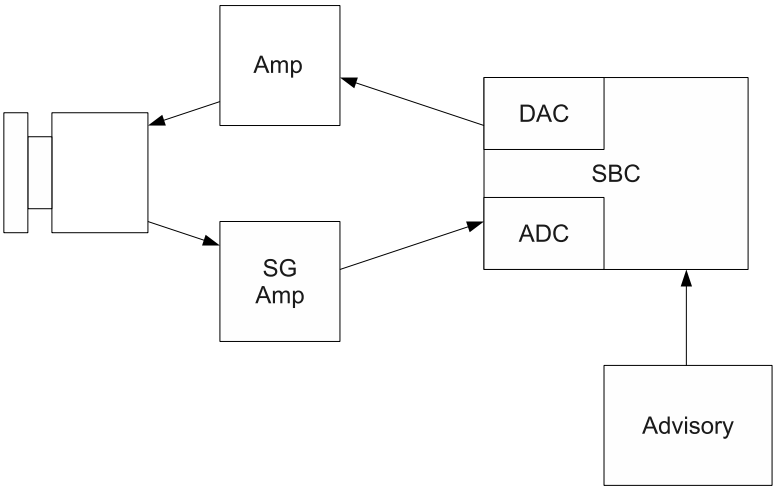

Figure 3: SBC setup for modulators

Due to the limited number of driver cards that can be run by the current FPGA, a new setup is proposed based around a single board computer (SBC) such as a PC104 or ARM based product. It could also use a FPGA with a softcore/ hardcore processor. This would free us from the PCI bus restriction and a single (or multiple) multi-channel DAC(s) could be used for waveform generation. Using a SBC over a FPGA would have to be looked into. The advantage of an FPGA is its reconfigurable hardware and timing. The modulators only need a driver and a sampler though the driver needs accurate timing, phasing and to be able to adjust the output rate. If the SBC can handle the timing, it should be a cheaper option than the FPGA.

The amplifier would have to scale the generated waveform to the needed amplitudes while still providing enough current to drive the modulator if the driver did not. An off-the-shelf amplifier exsists but is rather pricey and bulky and would require nine of them being purchased. An in-house solution could be looked at as well as other amplifiers off-the-shelf ones.